

IN THE CLAIMS:

Cancel claims 10 and 13.

Please amend the claims as follows:

1. (Three Times Amended) A semiconductor device having at least one memory cell having a capacitor cell formed of multiple layers of glass, said capacitor cell having a side wall surface, comprising:

at least one layer of boro-phospho silicate glass; [and]

at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of said at least one layer of boro-phospho silicate glass;

at least one layer of dielectric material covering at least the side wall surface of said capacitor cell; and

at least one electrode layer deposited over at least a portion of the at least one layer of dielectric material.

2. (Twice Amended) A semiconductor device having at least one memory cell having a capacitor cell formed of multiple layers of glass, said capacitor cell having a side wall surface, comprising:

a plurality of layers of boro-phospho silicate glass; [and]

a plurality of layers of germanium boro-phospho silicate glass, at least a portion of at least one layer of said plurality of layers of germanium boro-phospho silicate glass contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass;

at least one layer of dielectric material covering at least the side wall surface of said capacitor cell; and

at least one electrode layer deposited over at least a portion of the at least one layer of dielectric material.

3. (Previously Twice Amended) A semiconductor device having at least one memory cell having a capacitor cell formed of multiple layers of glass, said capacitor cell having a side wall surface, comprising:

a plurality of layers of boro-phospho silicate glass; and

a plurality of layers of germanium boro-phospho silicate glass, each layer of said plurality of layers of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

4. (Previously Twice Amended) A semiconductor memory device having at least one memory cell having a capacitor cell formed of multiple layers of glass, said capacitor cell having a side wall surface, comprising:

at least one layer of boro-phospho silicate glass; and

at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of said at least one layer of boro-phospho silicate glass.

5. (Twice Amended) A semiconductor memory device having at least one memory cell having a capacitor cell formed of multiple layers of glass, said capacitor cell having a side wall surface, comprising:

a plurality of layers of boro-phospho silicate glass; and

a plurality of layers of germanium boro-phospho silicate glass, at least a portion of at least one layer of said plurality of layers of germanium boro-phospho silicate glass contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass;

at least one layer of dielectric material covering at least the side wall surface of said capacitor cell; and

at least one electrode layer deposited over at least a portion of the at least one layer of dielectric material.

6. (Three Times Amended) A semiconductor memory device having at least one memory cell having a capacitor cell formed of multiple layers of glass, said capacitor cell having a side wall surface, comprising:

a plurality of layers of boro-phospho silicate glass; and

a plurality of layers of germanium boro-phospho silicate glass, each layer of said plurality of layers of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass;

at least one layer of dielectric material covering at least the side wall surface of said capacitor cell; and

at least one electrode layer deposited over at least a portion of the at least one layer of dielectric material.

7. (Three Times Amended) A semiconductor memory device having at least one memory cell having a capacitor cell formed of multiple layers of glass, said capacitor cell having a side wall surface, comprising:

at least one capacitor cell having a portion thereof formed by at least one layer of boro-phospho silicate glass and at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of said at least one layer of boro-phospho silicate glass;

at least one layer of dielectric material covering at least the side wall surface of said capacitor cell; and

at least one electrode layer deposited over at least a portion of the at least one layer of dielectric material.

8. (Twice Amended) A semiconductor memory device having at least one memory cell having a capacitor cell formed of multiple layers of glass, said capacitor cell having a side wall surface, comprising:

at least one capacitor cell having a portion thereof formed by a plurality of layers of boro-phospho silicate glass and a plurality of layers of germanium boro-phospho silicate glass, at least a portion of at least one layer of said plurality of layers of germanium boro-phospho silicate glass contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass;

at least one layer of dielectric material covering at least the side wall surface of said capacitor cell; and

at least one electrode layer deposited over at least a portion of the at least one layer of dielectric material.

9. (Twice Amended) A semiconductor memory device having at least one memory cell having a capacitor cell formed of multiple layers of glass, said capacitor cell having a side wall surface, comprising:

at least one capacitor cell having a portion thereof formed by a plurality of layers of boro-phospho silicate glass and a plurality of layers of germanium boro-phospho silicate glass, each layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass;

at least one layer of dielectric material covering at least the side wall surface of said capacitor cell; and

at least one electrode layer deposited over at least a portion of the at least one layer of dielectric material.

10. Canceled.

11. (Twice Amended) The memory device of claim 9 [10], wherein said at least one dielectric layer comprises one of  $\text{Si}_3\text{N}_4$ ,  $\text{Ta}_2\text{O}_5$ , or BST.

12. (Twice Amended) The memory device of claim 9 [10], wherein said conductive layer comprises Si-Ge.

13. Canceled.